AMENDMENTS

Amendments to the Specification:

Please replace paragraph [0024] with the following amended paragraph:

[0024] The DSE 253 of link layer device 250 may be used to multiplex the data transmitted on bus 201. The NSE 254 of link layer device 250 may perform data route-table look-ups. In one embodiment, NSE 254 may be, for example, a content addressable memory (CAM) device. In an alternative embodiment, the operations of the NSE 254 may be performed by other devices, for example, a random access memory (RAM) with a hashing function performed in the processing device 251. The NSE 254 may also serve as a server-load balancer, which takes incoming traffic from the Internet and distributes the processing load among a number of servers. Memory 252 of link layer device 250 may ~~included~~include a random access memory (RAM), or other dynamic storage devices, for storing information (e.g., packets) and instructions to be executed by processing device 251 of link layer device 250. The memory 252 of link layer device 250 may be used for storing temporary variables or other intermediate information during execution of instructions by processing device 251. The memory 252 of link layer device 250 may also include a read only memory (ROM) and/or other static storage ~~device~~devices for storing static information and instructions for processing device 251 of link layer device 250. It should be noted that link layer device 250 may also include other components that have not been illustrated. It should be noted that the components of link layer device 250 have been shown with separate components. In an alternative embodiment, one or more of the components of link layer device 250 may be combined with other components into one or more integrated circuits.

Please replace paragraph [0038] with the following amended paragraph:

[0038] Figure 5 illustrates one embodiment of a method for packet processing. The framer 240 may be initialized and ready to receive data from the link layer device 250, step 501. Data read request sent on line 453 is generated by the framer engine 350 and

sent to the request modifier circuitry 431, step 502. The data read request may be passed to the input FIFO 320 as modified data read request 450 by the request modifier circuitry 431, step 503. Data is sent on line 213 from the link layer device 250 to the input FIFO 320 for protocol processing, step 504. Data modifications are made in the encapsulator engine 430, step 505. Data modifications made during this step may include but are not limited to processing the data in multiple stages of a pipeline, packing the data, inserting idle cells, and adding or deleting bytes at the header and/or trailer of the packet. Request modifier circuitry 431 determines if the output FIFO 340 is substantially full by the substantially full signal sent by the output FIFO 340 to the request modifier circuitry 431 on line 454, step 506. If the output FIFO 340 is substantially full then at least one or more of the data read request received on line 453 by the request modifier circuitry 431 may be masked, meaning the request modifier circuitry does not send a modified data read request on line 450 to the input FIFO 320, step 507. The method may continue to mask the data read requests received on line 453 by the request modifier circuitry 431 as long as the output FIFO 340 is substantially full. If the output FIFO 340 is not substantially full then the data read request sent on line 453 may be passed to the input FIFO 320 as modified data read request 450 by the request modifier circuitry 431, step 503. The method may continue to pass the data read requests received on line 453 by the request modifier circuitry 431 as long as the output FIFO 340 is not substantially full.

Please replace paragraph [0047] with the following amended paragraph:

[0047] In one embodiment, the total bytes of data being generated by the link layer device 250 is calculated by the pre-compute circuitry 633 and transmitted to the read request circuitry 631 on line 660. The read request circuitry 631 uses the total bytes of data to update a counter value in the request modifier circuitry 631. By updating the counter, request modifier circuitry 631 calculates a variation between an input data rate and a pre-determined output data rate. The input data rate is based on the total bytes of data received by the pre-compute circuitry 633 as a result of the number of data read requests that are generated by the framer engine 350. The pre-determined output data rate is based on the pre-determined output data bus width. After the request modifier circuitry 631 has

calculated the variation between the input data rate and the pre-determined output data rate, the request modifier circuitry 631 compensates for the variation by modifying the number of data read requests sent to the link layer device 250. The counter value may reflect the current variation in bandwidth (i.e., variation between the input data rate and the pre-determined output data rate) of the packet processing system 200. When the counter value of request modifier circuitry 631 becomes more than an upper threshold value (e.g., the positive value of the pre-determined output data bus width), which may indicate that too little data is being sent to the physical interface device 260 from the link layer device 250, the request modifier circuitry 631 may generate at least one additional data read request and send the additional data read request to the link layer device 250 to fetch additional data by way of the input FIFO 320 on line 650. The additional data read requests may be generated by the request modifier circuitry 631 during the idle cycles, or in other words, between the data read requests that are generated by the framer engine 350 at a pre-determined output data rate. If the counter value becomes less than a lower threshold value (e.g., negative value of the pre-determined output data bus width), which may ~~indicates~~ indicate that too much data is being sent to the physical interface device 260, the request modifier circuitry 631 may mask at least one or more of the data read requests received on line 653 from the output FIFO 340.

Please replace paragraph [0054] with the following amended paragraph:

[0054] Data modifications may be made in the encapsulator engine 632, step 707. Data modifications made during this step may include but are not limited to processing the data in multiple stages of a pipeline, packing the data, inserting idle cells, and adding or deleting bytes at the header and/or trailer of the packet. Request modifier circuitry 631 determines if the counter value is between two threshold values, the positive value of the pre-determined output data bus width and the negative value of the pre-determined output data bus width, step 708.